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Abstract

This paper reports on a Ku low-power integer-N phase locked oscillator designed to investigate the potentialities of a low-cost 130 nm CMOS technology for video broadcasting and radiometry applications. The design and the characterization of the prototype are described and the main performances are reported and compared to literature. The PLO generates an output tone in the 14.2 GHz to 15.1 GHz frequency range. The phase noise is −68.9 dBc/Hz for an offset frequency of 100 kHz from a 15 GHz carrier, and can be enhanced of about 20 dB. The circuit core sinks 23.7 mA from 1.2 V supply.

Keywords: Ku band, CMOS, DVBS, PLO, microwave radiometer

1. Introduction

Several mass market applications, as for example, Standard and High Definition TeleVision (SDTV and HDTV), interactive multimedia, data content distribution and professional TV applications use a portion of Ku band spectrum reserved for point to point and broadcasting satellite communications. Nowadays, in satellite receivers, the signal is picked up by the dish antenna and then amplified and down-converted by a low noise front-end. This block is frequently built using discrete compound semiconductor High Electron Mobility Transistors (HEMT) and Dielectric Resonator Oscillators (DRO), as well. This discrete approach is expensive due to components, assembling operations, and the resonator manual tuning [1]. A silicon-based monolithic integrated receiver offers advantages in term of cost and size, specially when an integrated oscillator is used to replace the DRO. Nevertheless,

performance limitations of integrated solutions are still restricting this kind of solution for penetrating high frequency mass market applications such as Digital Video Broadcasting Satellite (DVB-S) [2]. Some efforts have led to several prototypes as a monolithic 0.8 µm bipolar technology Low Noise Block (LNB) by STMicroelectronics [1], and more recently, a 0.25 µm SiGe:C commercially available BiCMOS technology LNB reported by NXP Semiconductors [2]. Avoiding the use of bipolar transistors is of great interest as well, which is the aim of [3] and [4], where a 0.18 µm CMOS LNA/down-conversion mixer chain and a LNB, respectively are claimes. In all reported examples, the frequency synthesizer used to generate the local oscillator (LO) signal is a Phase Locked Loop (PLL). This kind of implementation requires a programmable frequency divider in the feedback loop. To easier demonstrate the potentiality of a technology for a given application where a local clock and/or a local frequency are required, the use of a Phase Locked Oscillator (PLO) is a good alternative because the frequency divider in a PLO exhibits a fixed modulus, making in this way easier its design.The present paper reports on the design and the characterization of a Ku-band PLO realized with a bulk 130 nm CMOS technology. The operation frequency was chosen so that to test its potentiality for both up-link ($12.9 \div 18.4$ GHz) and down-link ($10.7 \div 12.75$ GHz) frequency band. Particular attention has been paid on the phase noise which is the hardest specification to be satisfied. The modulations scheme (APSK) adopted in DVB-S standard exhibits indeed a round constellation where excessive rotational errors due to excessive phase noise would produce a burst of error [5]. The PLO can be also used as local oscillator in the architecture of a microwave radiometric front-end [6]. Several applications in the microwave radiometry field, such as industrial harsh plants, where conventional sensors can not be employed, or automotive safety, require cost and size reductions of the radiometer. For example, in order to keep low the cost, the emitted black-body radiation is usually detected with a low cost printed antenna array [6, 7], which size depends on the operation frequency. A PLO working at higher frequency allows therefore a reduction in the antenna size. For a 8×8 array patch-antenna with a gain of 25 dB, when the operation frequency moves from X-band to Ku-band, as in the present case, the antenna area shrinks of 2.5 times, from $10 \times 10\,\text{inch}^2$ to $6.3 \times 6.3\,\text{inch}^2$ [8]. Microwave radiometry is considered also an interesting solution for wild fire detection. In order to minimize the maintenance cost of the batteries, the microwave radiometer collocated in each node of the smart sensor network distributed on the wild area should be energy independent

as much as possible, exploiting renewable energy sources, as integrated microphotovoltaic cells or harvesting circuits [9]. Dissipated power reduction is therefore a further parameter of paramount importance. Using, as in this case, low power technology allows to solve this constraint, making easier to target the energy independence of each node of the smart sensor network. When bias voltage moves from a 3.3 V of a 0.35 µm technology to a 1.2 V of a 130 nm technology, a significant reduction of the dissipated power has to be expected. Therefore, the use of a higher operation frequency and more scaled technology with respect to those reported in [6] allows to address the above discussed advantages of reduction in size and dissipated power. The present paper is organized as follows. Section 2 gives brief description of the used technology. The PLO architecture and the design of each building block are described in Section 3 and 4, respectively. Experimental results are summarized in Section 5 followed by some considerations in Section 6. Finally conclusions are drawn in Section 7.

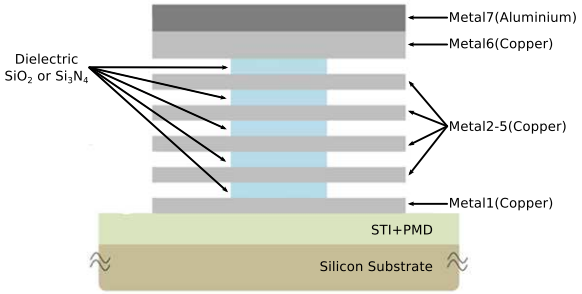


Figure 1: 130 nm CMOS STM technology (HCMOS9GP).

2. IC Technology

The circuit is designed to fit with the commercial HCMOS9GP technology from STMicroelectronics. It is a triple well bulk CMOS technology with multiple voltage threshold transistors, for low leakage or high speed purposes, featuring an effective gate length of 130 nm. As shown in Figure 1, the back-end features six copper layers with low-k inter-level dielectric and one aluminium layer on top [10], [11], [12]. The bias supply is typically 1.2 V even if the 2.5 V option is also available [11]. For the present design, low leakage, low threshold voltage transistors have been used with a supply voltage of 1.2 V. Several kinds of resistors are also available, as diffusion, salicied or

unsalicied poly, and high resistivity poly resistors [13]. MIM capacitors, spiral inductors, and varactors are also available.

3. PLO Architecture

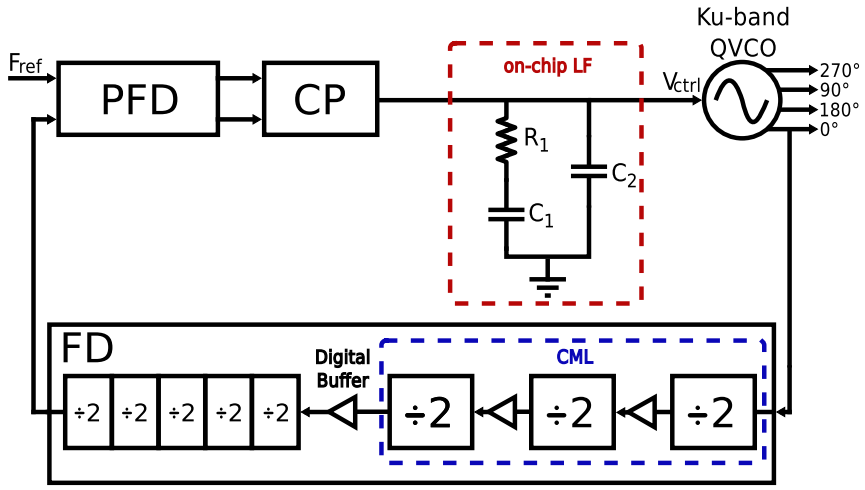


Figure 2: Phase Locked Oscillator Blocks Diagram.

Figure 2 depicts the building block diagram of the designed PLO. It is constituted by a Phase Frequency Detector (PFD), a Charge Pump (CP), a second order Loop Filter (LF), a Frequency Divider (FD), and a Quadrature Voltage Controlled Oscillator (QVCO). The difference with respect to an N-integer PLL is that the FD in the PLO exhibits a fixed modulus while in the PLL the FD is constituted by two blocks: the prescaler, a dual-modulus frequency divider guaranteeing a frequency resolution equal to the reference frequency, and a programmable section, usually implemented with down counters. It is worth here reminding that the design of the VCO/FD interface is the challenging step in the design flow of the loop, specially when the first block of the FD is the pre-scaler. The PLO architecture with its fixed modulus FD offers therefore the advantage of making a bit less critical the design of this interface. Once the potentiality of the addressed technology for a given application is demonstrated, efforts can be spent to design a programmable FD, to obtain a PLL from the PLO, in the case a PLL would be required.The frequency division ratio (256) of the FD is set for enabling the generation of a Ku-band tone from an external reference frequency f_{ref}

of about 60 MHz. The frequency divider is implemented as eight division-by-two stages. The first three stages are designed using a Current Mode Logic (CML) to achieve high operation frequency. Each CML stage is buffered in order to be able to drive the following divider stage. The division chain is completed with five low power digital frequency dividers realized with transmission gate registers. Because of the QVCO implementation, four output phases are available at PLO outputs. Finally, it is worth noticing that the loop filter is integrated on die for low cost considerations.

4. PLO Design

4.1. Quadrature VCO

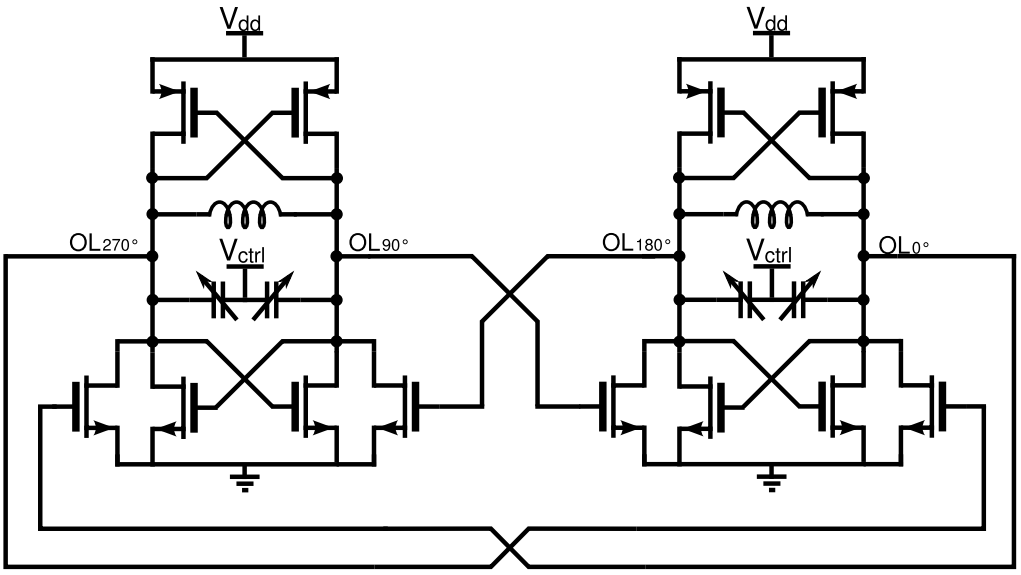


Figure 3: Schematic of the Quadrature VCO.

For generating signals in quadrature, the main techniques usually used are poly-phase filters, ring oscillators or frequency dividers. Nevertheless, in the present work two cross-connected symmetric LC VCOs has been preferred, because of their good phase noise performances.

The schematic of the QVCO is depicted in Figure 3 and was previously reported in [14]. Here some features and performances are quickly reminded; more details are available in [14]. The circuit is biased without current mirror to minimize the phase noise, the power consumption, and also to avoid any

automatic control circuit. All transistors exhibit the minimum gate length. The width of PMOS transistors must be wide enough to ensure robustness against fabrication tolerances. The octagonal inductor in the tank exhibits an inductance of about 290 pH and a maximum quality factor of 27. The tuning capability is achieved using two 20 fingers MOS varactors with a minimum gate length of 350 nm. For a carrier frequency ($f_{carrier}$) of 15 GHz, the dissipated power (P_{DC}) is 11 mW and the measured phase noise L(Δf) is -106 dBc/Hz for a carrier frequency offset (Δf) of 1 MHz.

4.2. Frequency Divider

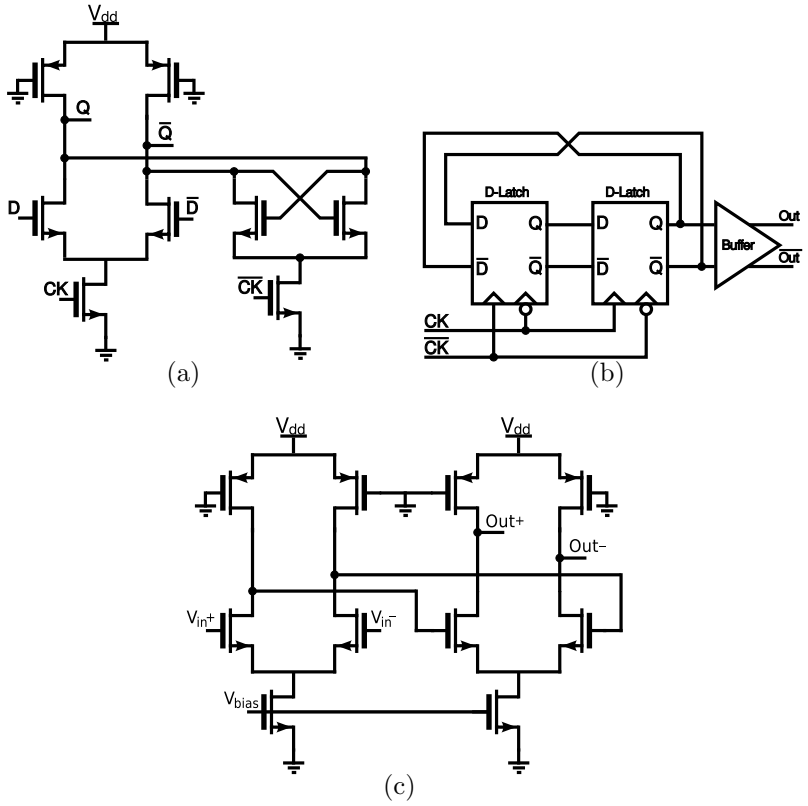


Figure 4: Schematic of: (a) CML latch, (b) Master-Slave divide-by-two frequency divider, (c) CML buffer

As previously stated, the frequency divider is composed of eight division stages. Because it operates at high frequencies, each of the first three division-by-two stages is implemented through the CML latch depicted in Figure 4(a).

The frequency division is carried out by two latches arranged in a master-slave configuration and closed in feedback, as depicted in Figure 4(b). The schematic of the output buffer required to drive the following division stage is shown in Figure 4(c) [15]. It is worth noticing here that the use of CML structures is well suited since their differential intrinsic topology contributes to reject the common mode noise injected from the supply and the substrate. Once translated in PLO performances, this rejection provides lower jitter and therefore lower phase noise [16]. In the present work the CML latch, and of course the resulting frequency division CML chain, is inductor-less, using PMOS transistors as loads to minimize the layout area of circuits. Because of the low voltage bias, the traditional tail current bias is removed [17]. The inductor-less solution sounds reasonable, since it can provide a 130 nm CMOS static frequency divider operating up to 45 GHz frequency. Inductors become mandatory when a 130 nm CMOS frequency divider should target millimeter wave frequencies [18]. Another design issue of paramount importance is the correct extraction and the minimization of parasitics at the interface between the VCO and the frequency divider. Unpredicted and/or false parasitics can translate into a frequency mismatch between the tuning range of the VCO and the sensitivity range of the frequency divider, making impossible the lock of the PLO. Therefore, a compact front-end of the frequency divider allows the optimization of this interface by reducing parasitics from the layout of this very critical interface. Because of this criticality the CML latch must be very carefully laid out. In order to assess the robustness of the circuit against technology dispersions, several post-layout simulations have been carried out under RC parasitic worst case of the VCO/FD interface and for several corner cases of transistor transconductance values. Figure 5 plots simulated output frequency versus input frequency of the first CML divider stage. A slope of 0.5 certifies the proper operation of this divide-by-two stage. Figure 5 shows that in the 6 GHz to 16 GHz frequency range, the CML divider stage is able to correctly work not only under the typical corner case (TT) but also under the Slow-Slow (SSA) and the Fast-Fast (FFA) corner cases, i.e. when the transistor transconductance is lower and higher than its typical value, respectively. Note that the frequency range where the circuit correctly works is larger (narrower) than the typical case when the transistors are fast (slow). The SSA case is therefore the most critical one. Similar simulations have been carried out for the other CML stages.

As far as the implementation of the last five division-by-two stages operating at lower frequency, dynamic CMOS latches are used as base cells where

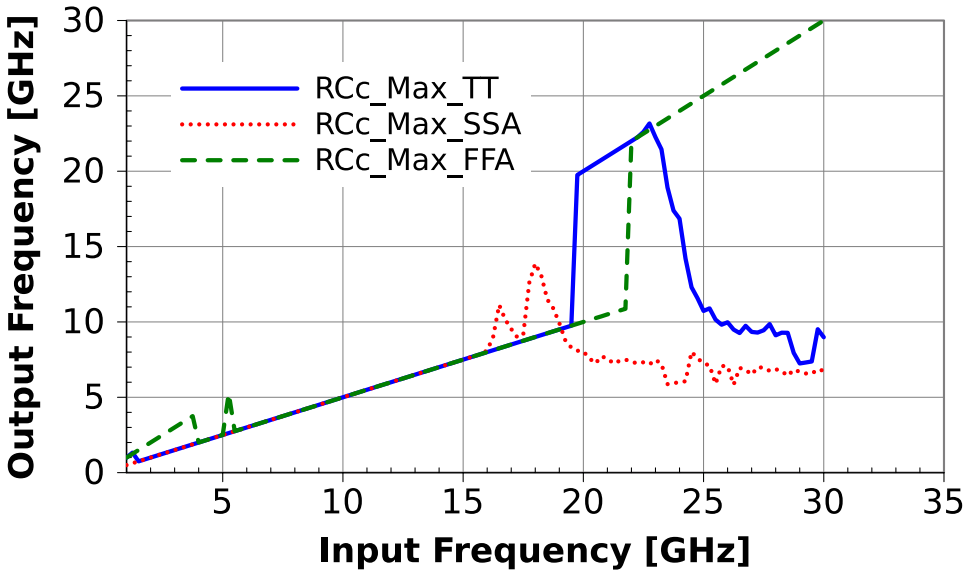


Figure 5: Output frequency versus input frequency of the first CML divide-by-two frequency divider for several corner cases under worst case parasitic extraction.

the transmission gates sample the input data and synchronize the transparent and opaque states. As depicted in Figure 2, a digital buffer, simply composed by the cascade of two inverters, interfaces the CML and the low frequency sections. The whole division chain exhibits a simulated power consumption of about 10.5 mW. The small size of the whole frequency divider (Figure 6) of $44 \times 154\,\mu m^2$ is mainly due to the inductor-less approach. Because in these conditions the connection between the QVCO output and the frequency divider can be very short (only few microns as pointed out in Figure 6), RLC parasitic components of the connection are minimized ensuring a good frequency matching between FD and QVCO.

4.3. Phase Frequency Detector, Charge Pump and Loop Filter

Figure 7(a) shows the schematic of the designed Falling-Edge (FE) PFD [19]. Thanks to the absence of a reset signal, as more traditional PFDs often requires, this configuration is dead zone free. This property leads to a better phase noise of the PLO. It is worth noticing that the True Single Phase Clock (TSPC) solution is dead zone free as well, but its implementation requires more transistors than the FE solution [19]. As it combines good phase noise and compact layout, the FE solution has been adopted in the

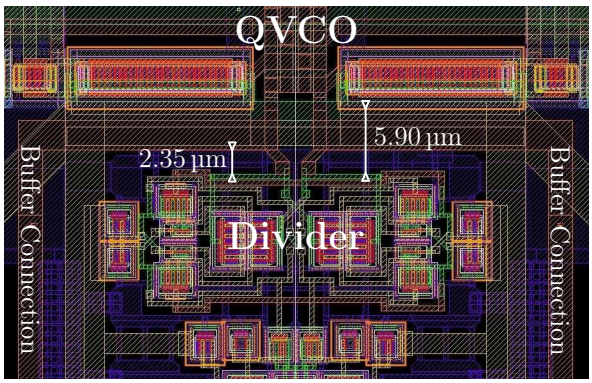


Figure 6: Detailed layout of the interface between the QVCO and the frequency divider.

present work. Further advantages offered by this structure are low dissipated power and high speed operation. It is worth pointing out that to avoid dead zone and get a good linearity of the phase characteristic, the FE PFD should compare signals exhibiting the same duty cycle with a value in the range of 50 % [19], which is the case of the PLO reported in the present paper. Under these conditions, the simulated phase noise of the designed FE PFD is about −173.8 dBc/Hz at frequency offset of 1 MHz, outperforming the −168.8 dBc/Hz claimed in [19]. Moreover, it has to be pointed out that the PFD schematic depicted in Figure 7(a) exhibits a differential structure. This topology not only makes the PFD robust against common mode noise sources but also provides up and down signals in both true and false forms, so that a differential CP can be driven.

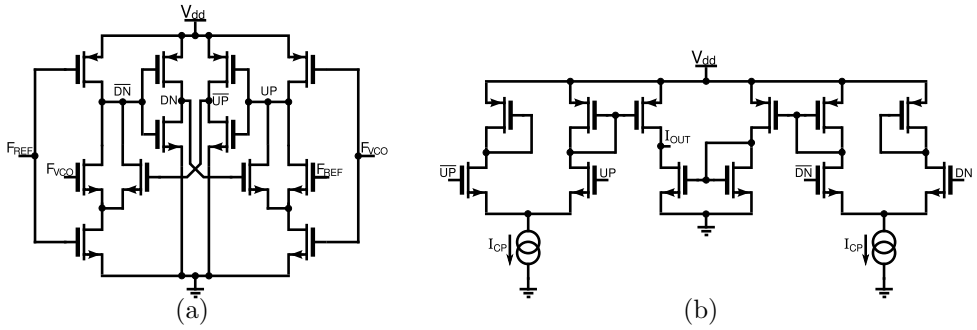


Figure 7: Schematic of the designed PFD (a) and charge pump (b).

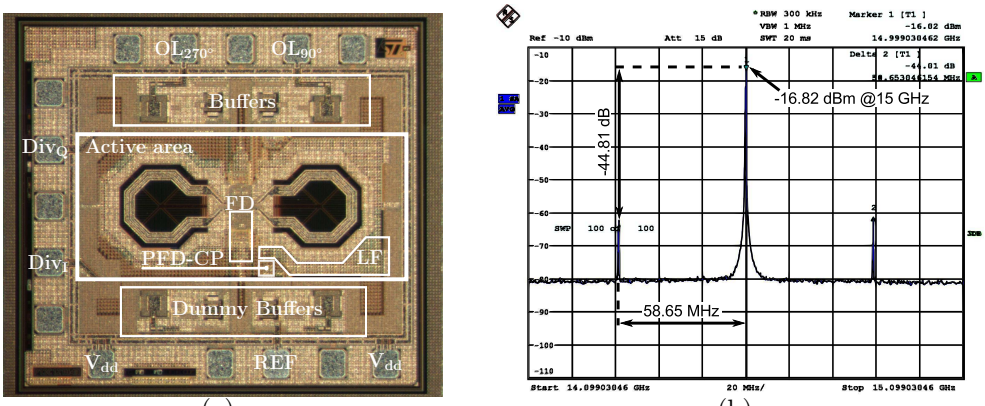
A differential topology is selected for the CP, which is able to improve

the common mode noise rejection [16]. The schematic of the designed CP is shown in Figure 7(b). Longer channel transistors are used in the current mirror to improve the current matching, as much as possible [20]. Finally, as known, the values of capacitance and resistance implemented in the loop filter (see Figure 2) depend on the desired open loop gain. More precisely, the capacitances are directly proportional to $K_\varphi \cdot K_{VCO}/(\omega_{BW})^2 \cdot N$, where $K\varphi$ is the gain of the CP, ω_{BW} the bandwidth of the PLO, and N is the division ratio of the frequency divider. Considering $K_\varphi = I_{CP}/2\pi$ where I_{CP} is the CP current, values of the capacitances are also directly proportional to this current. Hence, the size of the loop filter is kept small by setting I_{CP} to 25 µA. This low current value allows a second order loop filter to be integrated on chip ($C_1 = 44\,\text{pF}$, $R_1 = 27.09\,\text{k}\Omega$ and $C_2 = 3.39\,\text{pF}$). The resulting bandwidth and phase margin are 500 kHz and 60 degrees, respectively. To shrink the filter size as much as possible, polysilicon n-well capacitors are used for their higher capacitance-area ratio.

5. Experimental Result

Figure 8(a) shows the microphotograph of the fabricated prototype where each building block of the PLO is highlighted. Note in higher chip side the buffers driving the 50 Ω load of the external instrumentation.The GSGSG pads for the differential RF output ($\text{OL}_{90°}$, $\text{OL}_{270°}$) are also visible on the top of the chip. To keep the circuit as symmetric as possible for the best balanced operation of the QVCO, two dummy buffers are connected on both other RF outputs. These outputs are not available on pads for experimental test simplification. Both pads on the left are implemented for the measurement of the frequency divider output signals (Div_Q and Div_I). On the bottom, pads are visible for the reference signal and power supply. The size of the whole chip is $920 \times 1010\,\mu\text{m}^2$, pad enclosed. The PLO active area without buffers occupies an area of about $450 \times 900\,\mu\text{m}^2$, which is quite compact.

For sake of test simplification and measurements quality, the die is mounted on a PCB test board. The bias pads as well as the reference low frequency pad are wire-bonded to interconnection lines. High frequency output signals are measured through microwave coplanar probes. Thanks to this experimental set-up only one differential RF probe was required. The bias was correctly filtered with several microcapacitors located as close as possible to the die. The bias voltage was supplied by a TTi Thurlby Thandar Instruments PL330 32V-3A Power Supply Unit. The measurements were carried



(a) (b)

Figure 8: (a) Die microphotograph of the fabricated PLO, (b) Measured output spectrum

out inside a Faraday cage, in order to minimize possible interferences from parasitic signals. The differential output is applied to the single-ended input of the Rohde&Schwarz FSU67 Spectrum Analyzer by picking up only one signal and closing the other one on a 50 Ω load. The tuning external reference frequency is obtained from the Marconi instruments 2042 low noise signal generator (10kHz ÷ 5.4GHz). Figure 8(b) shows the measured spectrum. By sweeping the external reference frequency, a range of $f_{carrier}$ from 14.2 GHz to 15.1 GHz was observed, which matches the expected tuning range. The PLO delivered a power of about −16.8 dBm on a 50 Ω load, and it was biased with a current of 23.7 mA from 1.2 V supplied voltage. The phase noise was measured using the Agilent Technology signal source analyzer E5052B (10 MHz ÷ 7 GHz) associated with the microwave downconverter E5053A (3 GHz ÷ 26.5 GHz). Figure 9 shows the measured phase noise (red curve) for $f_{carrier} = 15$ GHz in the frequency span Δf from 10 Hz to 40 MHz. The figure shows that the PLO exhibited a phase noise $L(\Delta f) = -68.9$ dBc/Hz @ $\Delta f = 100$ kHz, $L(\Delta f) = -86.3$ dBc/Hz @ $\Delta f = 1$ MHz and $L(\Delta f) = -122.2$ dBc/Hz @ $\Delta f = 10$ MHz.

6. Discussion

Figure 9 shows a very good agreement between measured (red curve) and simulated (dotted blue curve) phase noise, indicating that the PLO correctly works. The simulated spectrum is obtained by taking into account the single contribution to the phase noise of the QVCO, the frequency divider, the

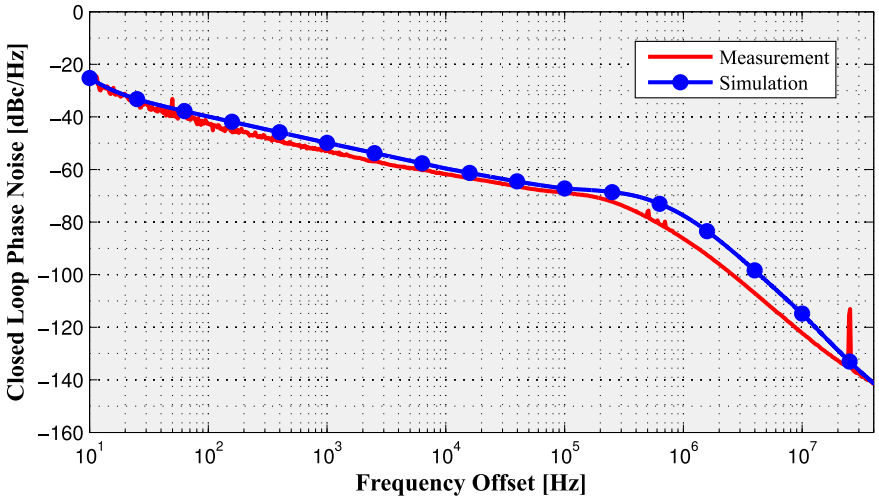


Figure 9: Comparison between measured and simulated phase noise.

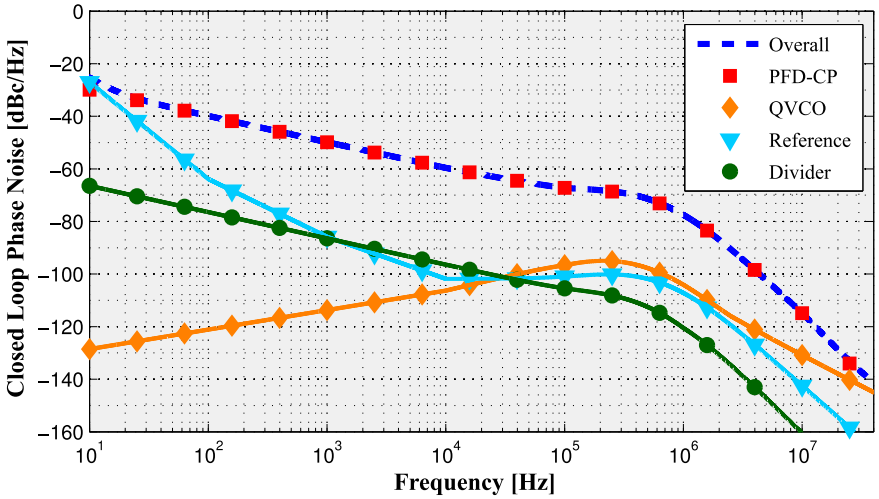


Figure 10: Simulated closed loop phase noise contributions.

PFD, and the CP. The contribution of each building block is simulated as in lock condition at transistor level and then introduced in a linear model of the PLO described using MATLAB® code and Simulink® models. With the transfer functions of this linear model and the noise contributions of each building block as an input, the developed tool computes both the open and

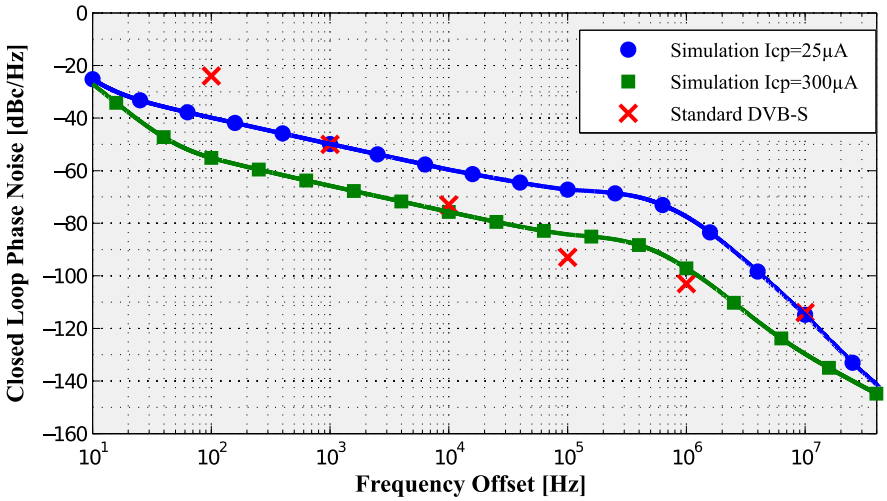


Figure 11: Comparison between the simulated phase noise with 25 µA and 300 µA charge pump current; red symbols are the DVB-S standard phase noise mask.

closed loop responses together with the loop design specification, the zero-pole information, and the phase noise spectra as well [21]. Each simulated phase noise contribution is reported in Figure 10, where the contribution of the reference signal is reported (sky-blue curve), as well. From these results, the PFD/CP block can be identified as the main contributor to the PLO overall phase noise.

In order to discriminate between PFD and CP, the PFD phase noise performance has been investigated using the following Figure-of-Merit for PFD ($\mathrm{FoM_{PFD}}$) reported in [22]:

$$\mathrm{FoM_{PFD}}(dBc/Hz) = L(\Delta f) - 20\log_{10} N - 10\log_{10} f_s \qquad (1)$$

where N is the division ratio of the frequency divider and f_s the external reference frequency. Using this $\mathrm{FoM_{PFD}}$ to compare the performances with literature allows to find the circuit section that must to be improved; in our case this part resulted to be the CP. Then, further investigation on the CP phase noise was carried out. As indicated in [23], the phase noise contribution of the CP is referred to the PLL input by dividing the total average noise at the CP output by the gain K_φ of this device. The following phase noise expression is derived in [23]:

$$\theta_n = 2\pi \sqrt{\left[\frac{2K\mu}{L^2\, f\, I_{CP}} + 4kT\left(\frac{2}{3}\right)\sqrt{\frac{2\mu\, C_{OX} W}{I_{CP}^3\, L}}\right] \cdot \left(\frac{t_{CP}}{T_0}\right)} \qquad (2)$$

where K is a proportionality constant depending on the process, L is the channel length of the CP transistors, μ is the channel electron mobility, and t_{CP} is the interval time during which both current sources of the charge pump are on during each period T_0. Equation (2) indicates that, even if a low maximum value of I_{CP} allows lower total average noise, as reported in [16], for lower phase noise a higher I_{CP} value is better [23]. Equation (2) indeed shows that the phase noise is inversely proportional to I_{CP}. Figure 11 compares two phase noise spectra simulated for the previous I_{CP} value of 25 µA and for a higher value of 300 µA. These spectra are then compared with the DVB-S standard phase noise limits (red symbols) [5]. A phase noise reduction of about 20 dB is observable as a consequence of increasing I_{CP}, demonstrating the importance of the CP contribution to the overall PLO phase noise. Moreover, Figure 11 points out that the higher value $I_{CP} = 300\,\mu A$ moves the phase noise fair close to the limits set by the DVBS standard. In particular, the PLO phase noise is better than the standard for offset frequency lower than 10 kHz, and for offset frequency higher than 1 MHz. In the 10 kHz÷1 MHz offset frequency range, the obtained phase noise is fairly comparable with the standard. As already pointed out, since the capacitances are directly proportional to the gain of the charge pump, a trade-off between the loop filter size and the phase noise performance must be found. In particular, a $I_{CP} = 300\,\mu A$ would require to increase by a factor of about twelve ($C_1 = 527.7$ pF, $R_1 = 2.25\,k\Omega$ and $C_2 = 40.82$ pfarad) the value of the capacitances. For instance, the loop filter of the measured prototype (Figure 8(a)) occupies an area of about 15 800 µm^2 (0.016 mm^2); whereas for $I_{CP} = 300\,\mu A$, the occupied area of this filter increases to about 189 200 µm^2 (0.189 mm^2).

Even if the obtained phase noise performance have been previously compared with the DVB-S standard phase noise mask in terms of phase noise spectra, under a telecom point of view an evaluation of the noise performance in terms of integrated phase noise is also of interest, being closer related to the quality of the received constellation in the base band section. To this aim a comparison with other silicon-based PLLs already reported in the literature is carried out by using the following Figure-of-Merit [22]:

$$\mathrm{FoM_{PLL}}(dB) = 10\log_{10}\left[\left(\frac{\sigma_{t,PLL}}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right)\right] \tag{3}$$

where $\sigma_{t,PLL}$ is the RMS jitter and P_{DC} is the DC power consumption. When only the phase noise spectrum is reported, a short script, developed in Matlab code, computes the jitter through the following formula [22]:

$$\sigma^2_{t,PLL} = \frac{1}{2\pi^2 f^2_{carrier}} \int_0^\infty L_{PLL}(\Delta f) d\Delta f \cong \frac{1}{2\pi^2 f^2_{carrier}} \int_W L_{PLL}(\Delta f) d\Delta f \tag{4}$$

where L_{PLL} is the phase noise of the PLL and W is the finite offset frequency integration range. The used value of W for each reference is listed in Table 1. In the limits of the data available in each reference, efforts are made to keep W as uniform as possible (about $10\,\mathrm{kHz} \div 40\,\mathrm{MHz}$ frequency range), in order to get a homogeneous comparison. Figure 12 shows the computed results where each reference is related to the DC power consuming and jitter variance. Even if the operation frequency of the circuit (38 GHz) claimed in [24] is about two times the operation frequency addressed in the present work (15 GHz), reference [24] has been accounted for, because of the very low values of jitter and FoM.The FoM of the proposed PLO is well located in the comparison with the literature, since it is close to $-215\,\mathrm{dB}$ in the case of a $I_{CP} = 25\,\mu\mathrm{A}$ and falls down to about $-230\,\mathrm{dB}$ in the case of a $I_{CP} = 300\,\mu\mathrm{A}$. Figure 12 shows also the jitter variance limit (red line) calculated with equation (4) using the phase noise limit of the DVBS standard, previously depicted in Figure 11. One can see that the presented PLO comes closer to the two best performances [24], [25] and to the DVBS jitter limit when an increase of the loop filter silicon area is acceptable, in order to increase I_{CP}.

This is a very interesting result, because the fabricated PLO prototype demonstrates that a pure bulk CMOS technology, a 130 nm CMOS technology in the present case, exhibits very promising potentialities for the fabrication of a PLL compliant with the DVB-S standard.

A more detailed performances comparison is summarized in Table 1. Note the low power consumption of the PLO described in the present paper when the buffer contribution is neglected; its dissipated of 28mW is challenged only by the PLL reported in [25] and several times lower, between two and sixteen times, the power dissipated by the other PLLs. This result in addition with the small occupied silicon area give to the proposed PLO a large interest

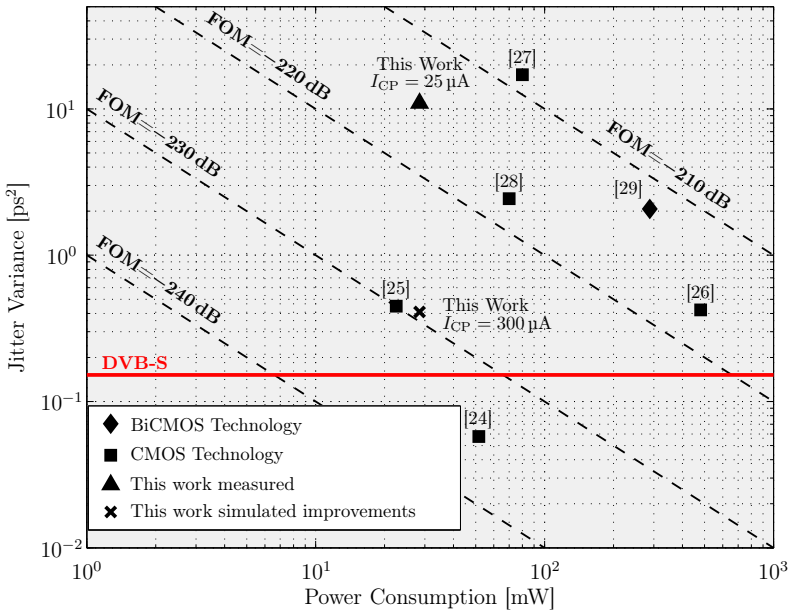


Figure 12: Jitter and power comparison between the PLO reported in this work and others PLL reported in the literature in term of FoM_{PLL}.

in the case of mobile and/or energy self-sustaining applications where the dissipated power should be kept as low as possible.

7. Conclusions

This paper reports on the design of a low-power integer-N PLO fabricated in a low cost 130 nm CMOS technology. The proposed PLO operates in the Ku-band, generating an output tone in the 14.16÷15.12 GHz frequency range. The power delivered to a 50 Ω load is about −16.8 dBm and the phase noise is −86.3 dBc/Hz for an offset frequency of 1 MHz and of −122.2 dBc/Hz for an offset frequency of 10 MHz. The PLO sinks 23.7 mA from 1.2 V supply. The discussion of the experimental data points out that the charge pump is the main responsible for the measured phase noise level. Once compared in terms of jitter with other silicon-based PLOs and PLLs reported in the literature, the PLO of this work is well aligned if the charge pump current is set to a value that keeps low the silicon area for the loop filter. For higher charge pump current the PLO performs better than a large number of the other

	This Work 1	This Work 2	[24]	[25]	[26]
Process	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm
Frequency [GHz]	15	15	38	20.05	19.2
Freq. Range [GHz]	14.2 ÷ 15.1	14.2 ÷ 15.1	37 ÷ 38.5	20.05 ÷ 21	17.6 ÷ 19.4
Supply [V]	1.2	1.2	1.2	1.5	1.3÷1.5
Power [mW]	28.43*	28.43*	51.6*	22.5	480.4
Chip Area [mm^2]	0.45 × 0.9*	0.45 × 1.3*	1.5 × 1.1	0.6 × 1	1.7
Phase Noise [dBc/Hz]	-68.9@100kHz -86.28@1MHz -122.3@10MHz	-84.3@100kHz -97.17@1MHz -129.7@10MHz	-85@100kHz -97.5@1MHz	-77@100kHz -98.5@1MHz -116.1@10MHz	-84@100kHz -101.2@1MHz -113.5@10MHz
Ref. Frequency	58.6 MHz	58.6 MHz	1.1875 GHz	78 MHz	600 MHz
Bandwidth [Hz]	500k	500k	15.625M	400k	≈4M
Filter/ Division_Ratio	Integrated/Fixed	Integrated/Fixed	Integrated/Fixed	Integrated/Progr	Integrated/Fixed
I_{CP} [µA]	25	300	250	70	-
Reported jitter rms [ps]	-	-	0.24	-	0.65
Calculated jitter rms [ps] (Integration Range)	3.31 (10kHz÷40MHz)	0.64** (10kHz÷40MHz)	0.36 (10kHz÷40MHz)	0.67 (50kHz÷40MHz)	0.78 (10kHz÷40MHz)
FoM [22]	-215.1	-229.3**	-235.3	-230	-216.9

	[27]	[28]	[29]	[30]
Process	CMOS 65 nm	CMOS 180 nm	SiGe:C BiCMOS 0.25 µm	SiGe:C BiCMOS 0.13 µm
Frequency [GHz]	20.88	15	15.75	20.76
Freq. Range [GHz]	19.44 ÷ 21.6	13.9 ÷ 15.6	14.25 ÷ 15.75	20.51 ÷ 21.27
Supply [V]	1.2 ÷ 1.8	1.8	2.5÷1.5	1.5
Power [mW]	80	70	288	40
Chip Area [mm^2]	1.6 × 1.9	1	0.7 × 0.8	0.84 × 0.57
Phase Noise [dBc/Hz]	-65@100kHz -100@1MHz -126@10MHz	-73@100kHz -103.8@1MHz	-68.66@100kHz -97.17@1MHz	-68.66@100kHz -97.17@1MHz
Ref. Frequency	36 MHz	71 MHz	250 MHz	81.1 MHz
Bandwidth [Hz]	≈70k	200k	≈3MHz	-
Filter/ Division Ratio	External/Progr	Integrated/Progr	Integrated/Progr	Integrated/Fixed
I_{CP} [µA]	-	600	-	100
Reported jitter rms [ps]	-	-	-	-
Calculated jitter rms [ps] (Integration Range)	4.14 (10kHz÷40MHz)	1.56 (10kHz÷40MHz)	1.44 (10kHz÷40MHz)	-
FoM [22]	-208.6	-217.7	-212.3	-

** Without buffers implemented for characterization purpose*
*** With I_{CP} = 300 µA*

Table 1: Performances comparison summary with other silicon-based PLL.

PLOs and PLLs, even if this high level of performances goes with an increase of the loop filter silicon area . These results demonstrate that a low-cost 130 nm CMOS technology is very promising for DVBS, where only discrete components or SiGe technologies have been employed until now. In addition, the reported prototype opens also the way to the fabrication of the front-end of a Ku-band microwave radiometer. For this application, the interest of the proposed PLO comes from the large reduction of the antenna size with respect to X-band radiometer, because of the higher operation frequency, and from its low dissipated power. The proposed PLO is therefore interesting for use in a smart sensor network for the detection of wild fire in outdoor environment. In this case, the low DC consumption is very welcome to supply

the electronics with a small dimension energy harvester. In summary, the PLO reported in the present work demonstrates that DVB-S compliant phase noise performance can come together with a low power dissipation in a PLL designed in a bulk low cost 130nm CMOS technology.

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